Claim Amendments

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (previously amended). A process for producing a doped semiconductor substrate, which comprises the following steps:

providing a semiconductor substrate;

producing a doping at a surface of the semiconductor substrate;

after producing the doping, applying a layer selected from the group consisting of a polycrystalline layer and an amorphous layer to the surface; and

carrying out a heat treatment step for producing an epitaxial layer and a buried doping.

Claim 2 (previously amended). The process according to claim 1, wherein a further amorphous layer that extends to a predetermined depth into the semiconductor substrate is produced by ion bombardment before a heat treatment step.

Claim 3 (original). The process according to claim 2, which comprises carrying out the ion bombardment with at least one ion type selected from the group consisting of germanium ions, silicon ions and noble gas ions.

Claim 4 (previously amended). The process according to claim 2, which comprises forming the further amorphous layer to have a thickness of between 500 - 1000 nm.

Claim 5 (original). The process according to claim 1, which comprises performing a rapid thermal annealing process before carrying out the heat treatment step.

Claim 6 (original). The process according to claim 5, which comprises carrying out the rapid thermal annealing process out at a temperature of between 1000° and 1100° C.

Claim 7 (original). The process according to claim 5, which comprises carrying out the rapid thermal annealing process for a time period of between 10 and 60 seconds.

Claim 8 (original). The process according to claim 1, which comprises forming the semiconductor substrate from silicon.

Claim 9 (original). The process according to claim 1, which comprises forming the polycrystalline layer and the amorphous layer from silicon.

Claim 10 (original). The process according to claim 1, which comprises producing the doping by an ion implantation process.

Claim 11 (previously amended). The process according to claim 10, which comprises carrying out the ion implantation process using ions selected from the group consisting of B, P, As, In and Sb ions.

Claim 12 (original). The process according to claim 1, which comprises depositing a poly/α layer using a low-pressure chemical vapor deposition process to the surface of the semiconductor substrate.

Claim 13 (original). The process according to claim 12, which comprises depositing the poly/α layer at a low temperature.

Claim 14 (original). The process according to claim 12, which comprising forming the poly/α layer to have a thickness between 20 nm to 40 nm.

Claim 15 (original). The process according to claim 12, which comprises carrying out a crystallization of at least one of the amorphous layer and the poly/α layer by performing a low-temperature step.

Claim 16 (original). The process according to claim 15, which comprises carrying out the low-temperature step at a temperature of between 600° C to 700° C.

Claim 17 (original). The process according to claim 15, which comprises carrying out a wet etching operation out after performing the low-temperature step.

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Claim 18 (original). The process according to claim 15, which comprises performing the crystallization at a same time as a formation of a gate oxide.

Claim 19 (original). The process according to claim 12, which comprises depositing the poly/α layer at a temperature of between 500° C and 600° C.

Claim 20 (original). The process according to claim 15, which comprises carrying out the low-temperature step at a temperature of 650° C.

Claim 21 (currently amended): A process for producing a ~~semiconductor substrate~~ MOS transistor with a buried doping, which comprises the following steps:

providing a semiconductor substrate;

producing a doping at a surface of the semiconductor substrate;

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after producing the doping, applying a layer selected from the group consisting of a polycrystalline layer and an amorphous layer to the surface;

subjecting the assembly to ion bombardment or to RTA processing with a rapid heat treatment to thereby destroy an oxide layer present between the semiconductor substrate and the polycrystalline or amorphous layer; and

subjecting the assembly to a heat treatment step for producing a monocrystalline layer and a buried doping from the layers and the semiconductor substrate for forming the MOS transistor.